Mixed Signal Techniques for RF Transceivers

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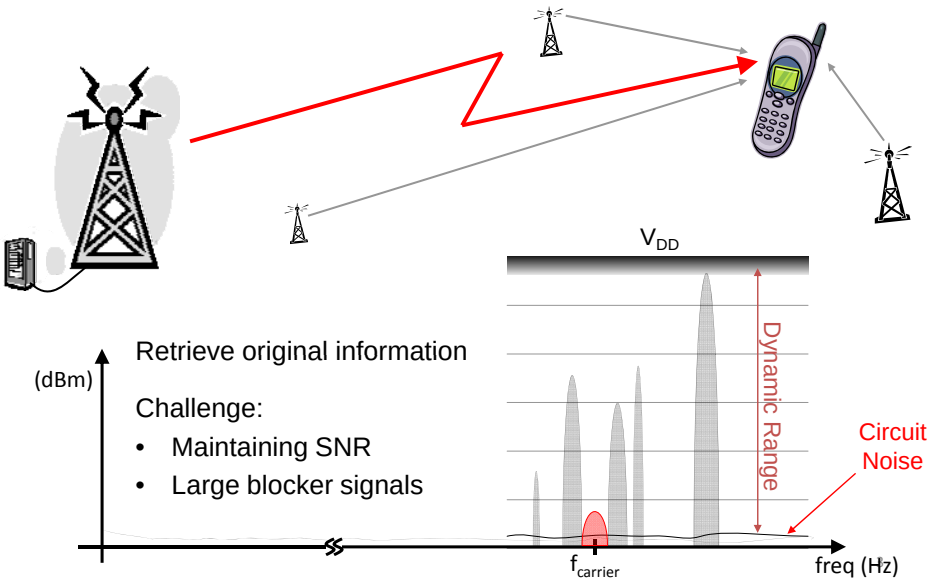
EE242 Guest Lecture, Spring 2009
April 29th, 2009

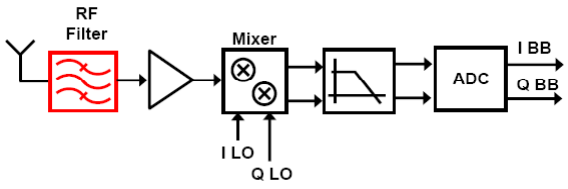
Outline

- RF Receivers: A Mixed-Signal Perspective
- Discrete-Time RF Receivers
- Sigma-Delta A/D Converters
  - Intro to Sigma-Delta Modulation
  - Sigma-Delta Converters in RF Receivers
- Mixed-Signal Techniques in RF Transmitter

Wireless Communication System

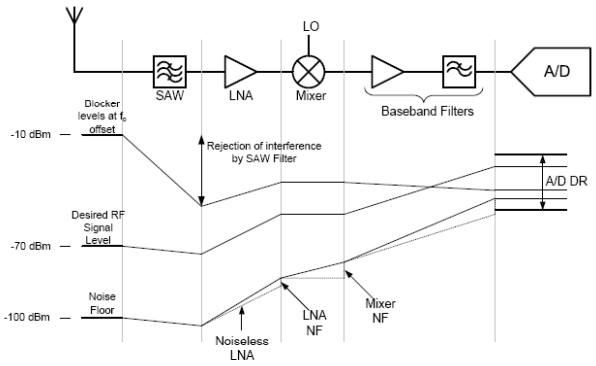


A Direct-Conversion Receiver



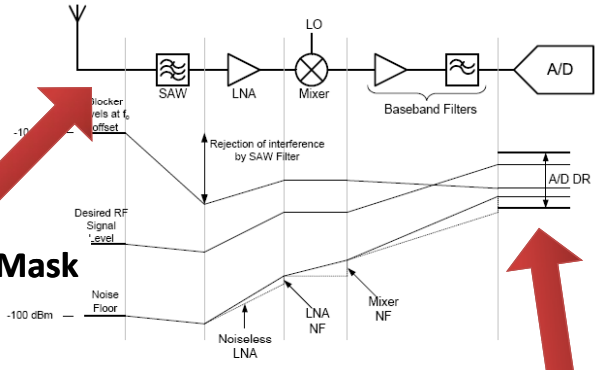
- **Mix – Amplify – Filter** → A/D Conversion
- Virtually all RF receiver today has an A/D
  - Complex modulation schemes to achieve spectral efficiency
  - Needs digital circuit to perform complex demodulation algorithm

RF Receiver : A Mixed-Signal Perspective



- A receiver ***pre-conditions*** an RF signal for A/D conversion

Deriving Requirements

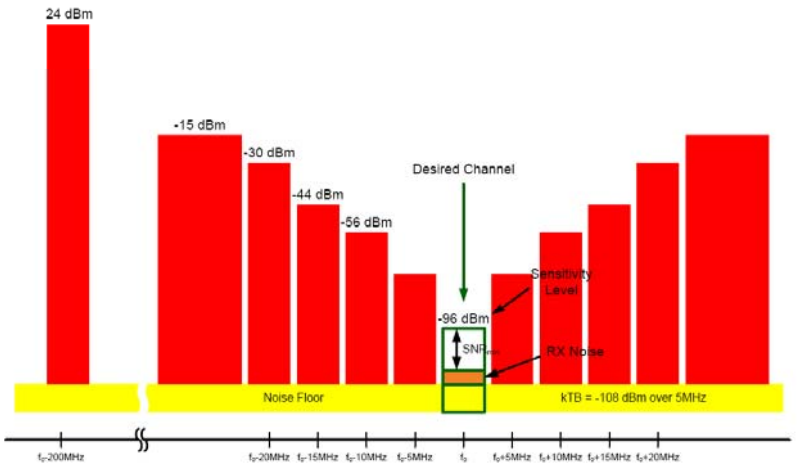


Blocker Mask

A/D Specifications

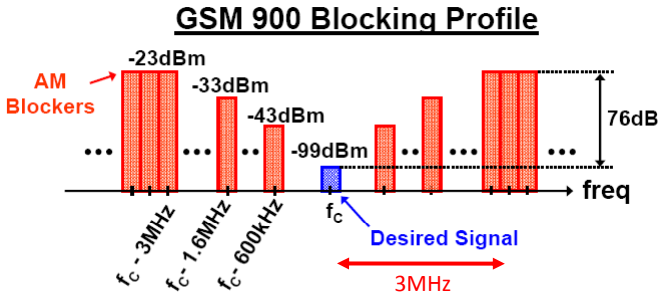
- System specifications for receiver is derived from the ***blocking mask*** and the choice of ***A/D converters***

UMTS Blocker Mask



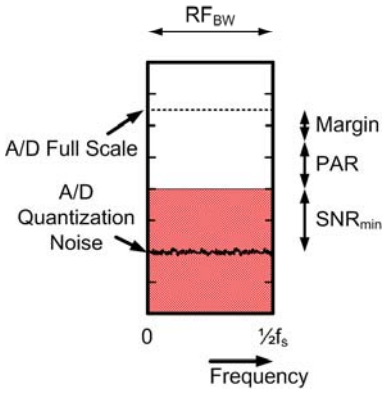
GSM Blocker Mask

Narrow-band signals



A/D Converters Specifications

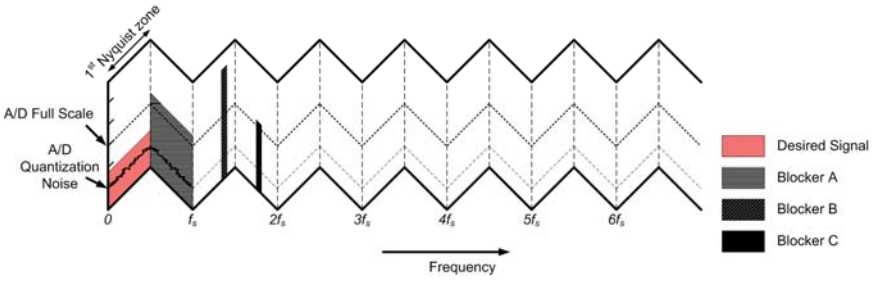
Sufficient Condition



- Nyquist Criterion
  - $F_s = 2xRF_{BW}$
  - Doesn't have to be at DC !
    (Beware of noise folding)
- Dynamic-range budgeting
  - SNR_{min} for successful decoding
  - Peak-to-average power ratio
  - Margin for other 'stuff'
    (intermods, leftover blocker signals, etc)

A/D Converters Specifications

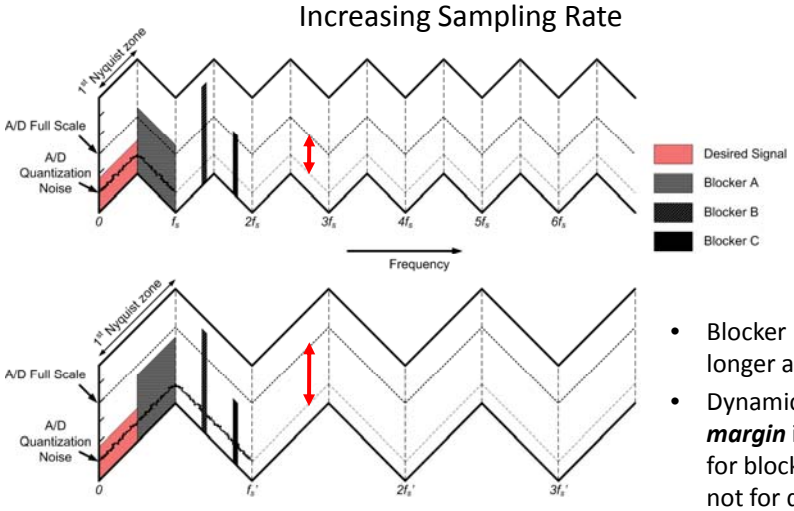
The Full Picture



- Desired signal is not in isolation
- Blocker signals will fold down due to a sampling operation (aliasing)
- Adjacent channels are especially hard to filter out

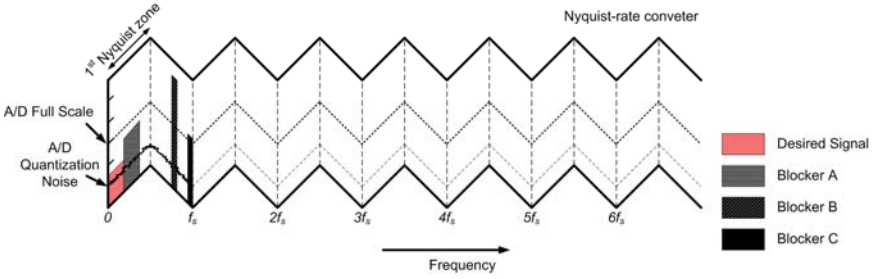
A/D Converters Specifications

Increasing Sampling Rate



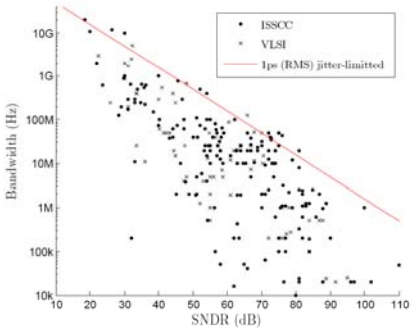
- Blocker B is no longer aliased
- Dynamic-range ***margin*** is allocated for blocker power, not for desired signal

A/D Converters Specifications

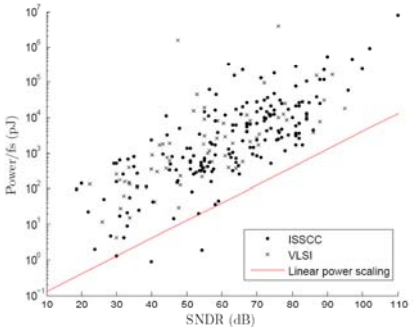


- Multiple stages of filters are needed in an RF receiver to eliminate aliases
- Increase A/D sampling-rate:
  - ✓ Relax anti-aliasing filter requirements
  - × Potentially an increase in A/D dynamic-range
  - × Increase in A/D power consumption

A/D FOM Survey



- What is achievable ?
- $1ps_{(RMS)}$ jitter seems to be the empirical limit



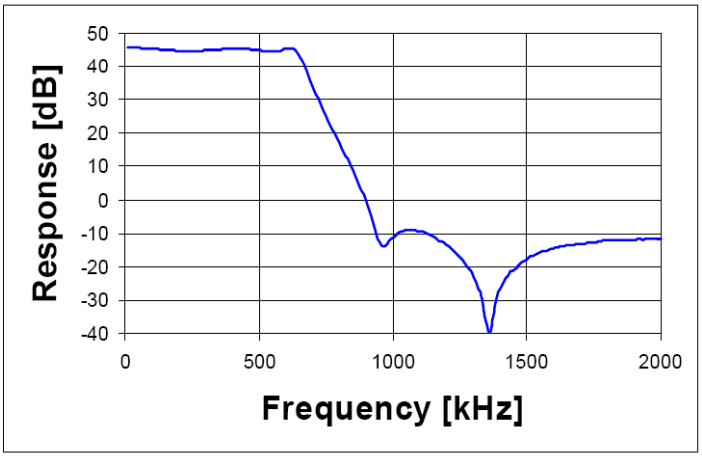
- 10x power for 20dB improvement in SNDR
- Trend deviate for high-res converters

B. Murmann, ADC Performance Survey

Pre-condition RF Signals: Summary

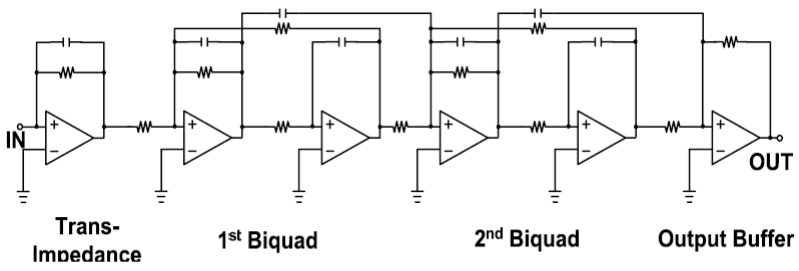
- Blockers are **BAD**:
  - Large magnitude will saturate circuits
  - It will alias down within A/D converter
- Role of baseband filters:
  - Limit dynamic range, filter out large blockers
    - Make life easier for succeeding blocks
  - It serves as an ***anti-alias filter*** for the A/D
- Better A/D → Less filter stages
  - Power optimization between filters and A/D

Example: CDMA Baseband Filter



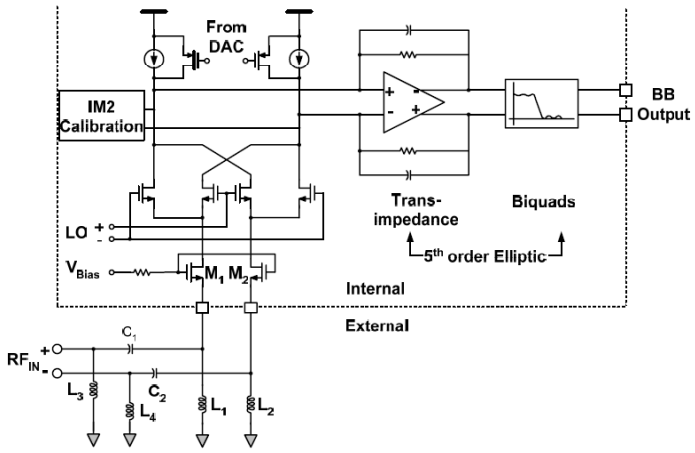
V. Aparin, ISSCC 2005

CDMA BB Filter: Implementation



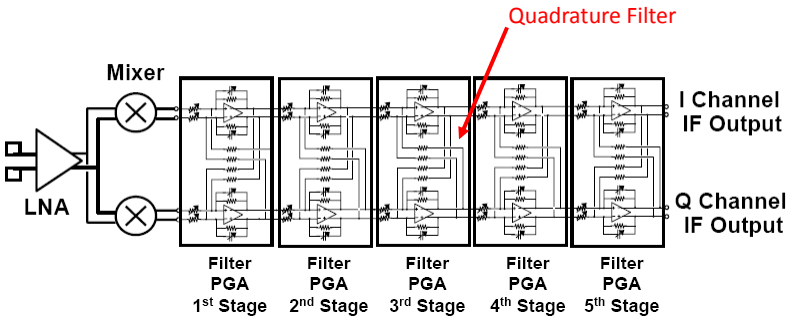
V. Aparin, ISSCC 2005

CDMA BB Filter: Mixer + 1 pole



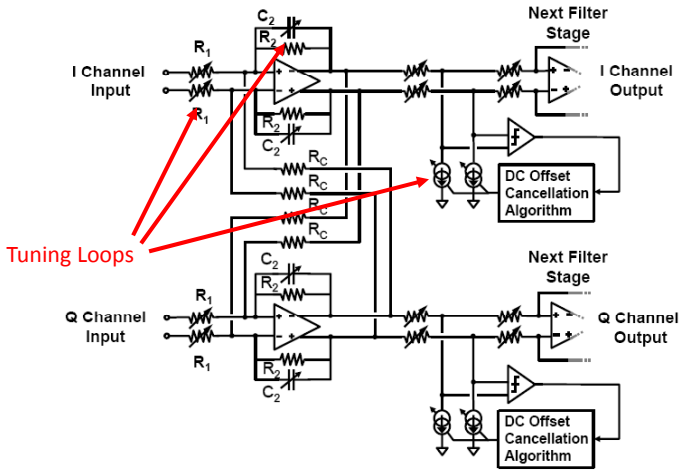
V. Aparin, ISSCC 2005

GSM BB Filter



O. Erdogan, J. Rudell, ISSCC 2005

GSM BB Filter

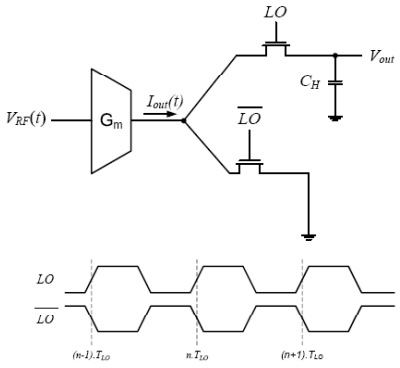


O. Erdogan, J. Rudell, ISSCC 2005

Discrete-Time Filters

- Advantages
  - Well-defined corner frequencies (Cap matching)
  - Corner frequencies are tunable (switch in/out caps)
  - Superior linearity
- Disadvantages
  - Sampled-data system → Aliasing
  - Operating speed is limited by OTA settling
  - Power consumption

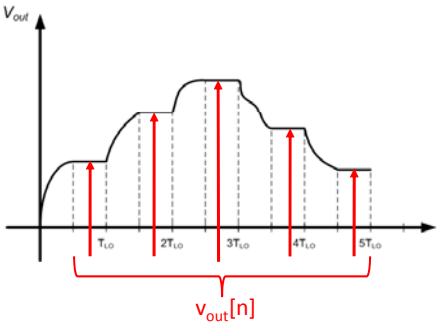
Sampling Mixer



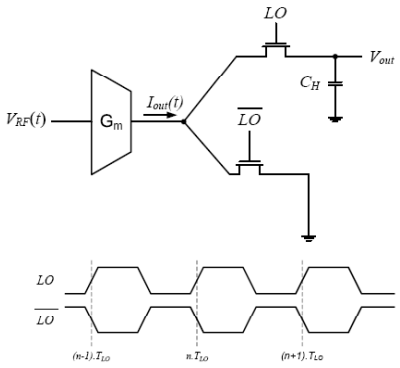
Single-balanced mixer with capacitive load

$$v_{out}[n] = \frac{q_{in}[n]}{C_H} + v_{out}[n-1]$$

$$q_{in}[n] = G_m \cdot \int_{nT_{LO}}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot d\tau$$



Sampling Mixer



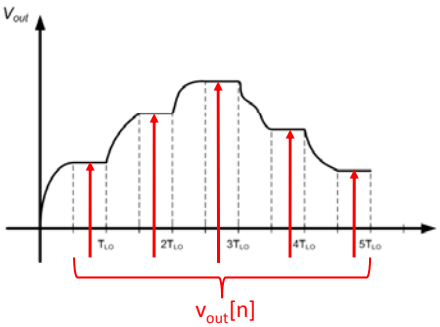
Single-balanced mixer with capacitive load

DT Integrator

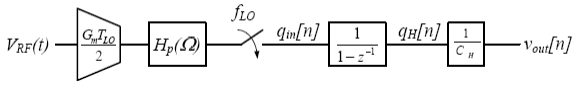
Charge Packets

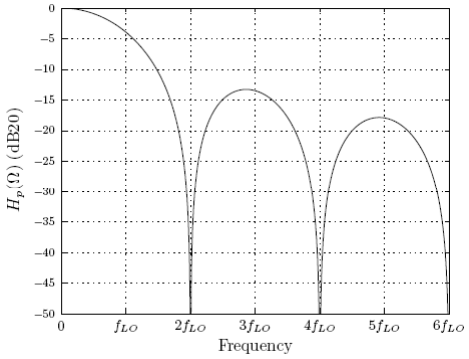
$$v_{out}[n] = \frac{q_{in}[n]}{C_H} + v_{out}[n-1]$$

$$q_{in}[n] = G_m \cdot \int_{nT_{LO}}^{nT_{LO}+\frac{T_{LO}}{2}} V_{RF}(\tau) \cdot d\tau$$



Sampling Mixer - Model



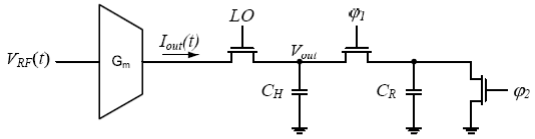


Sampling Mixer: Recap

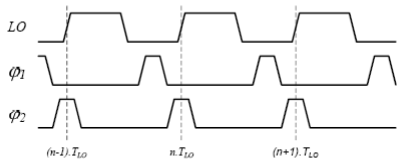
- Output of a mixer is ***discrete-time***
  - Needs to evaluate at the right time-instants
  - Slightly more complicated for double-balanced
- Mixer is a ***sampler***
  - Aliasing still happens with period of f_{LO}
  - Nulls on even harmonics due to nature of windowed-sampling
  - No need for another sample-and-hold amplifiers !

Lossy Integrator

Well-controlled corner frequency



$$q_H[n] = \alpha \cdot q_H[n-1] + q_{in}[n]$$



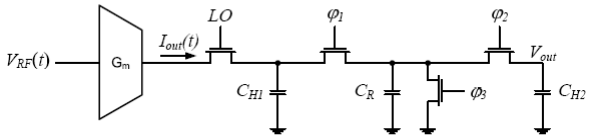
$$\frac{Q_H(z)}{Q_{in}(z)} = \frac{1}{1-\alpha z^{-1}}$$

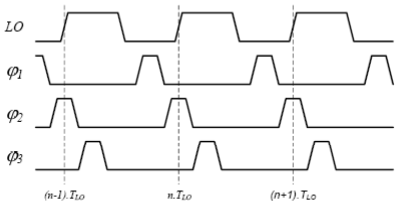
$$\alpha = \frac{C_H}{C_H + C_R}$$

α controls corner-frequency

$$G_c = \underbrace{\frac{G_m T_{LO}}{2}}_{\substack{V\to Q \\ \text{conv. gain at DC}}} \cdot \underbrace{\frac{\pi}{2}}_{H_p(f_{LO})} \cdot \underbrace{\frac{1}{1-\alpha_1}}_{\substack{DT\ \text{integrator} \\ \text{gain at DC}}} \cdot \underbrace{\frac{1}{C_H}}_{\substack{Q\to V \\ \text{conversion}}}$$

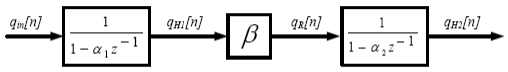
Higher-Order IIR Filtering



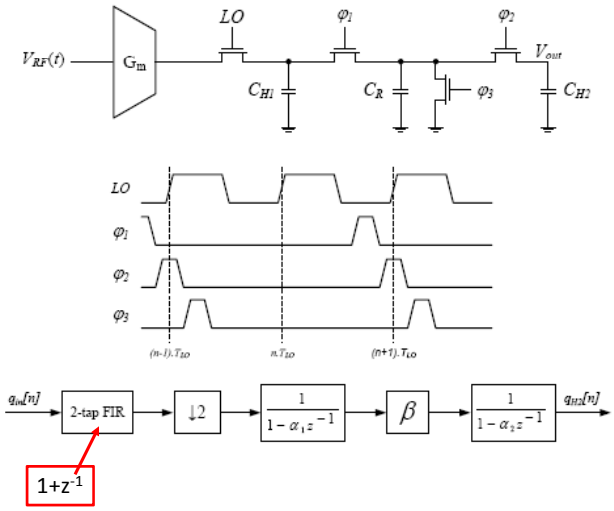


$$\alpha = \frac{C_H}{C_H + C_R}$$

$$\beta = \frac{C_R}{C_{H1} + C_R} = 1 - \alpha$$

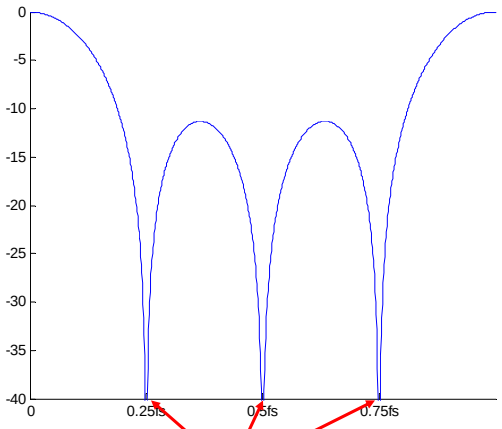


Sample-Rate Down-conversion



Moving-Average Filters

'Ideal' Anti-alias filtering

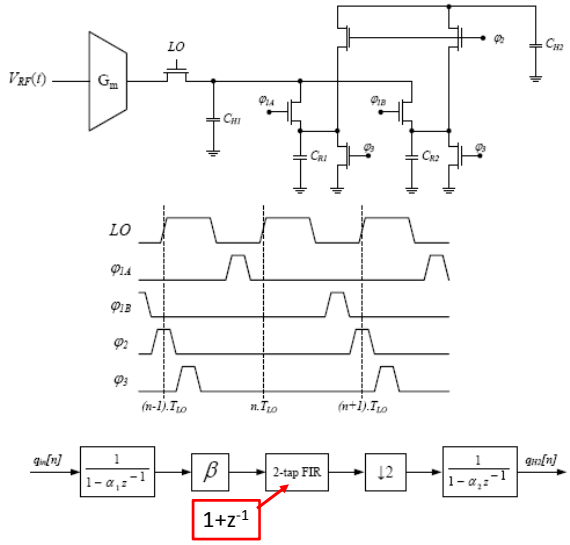


Downsample-by four

FIR : $H(z) = 0.25[1+z^{-1}+z^{-2}+z^{-3}]$

Nulls exactly at potential aliases
(assuming narrow-band signals)

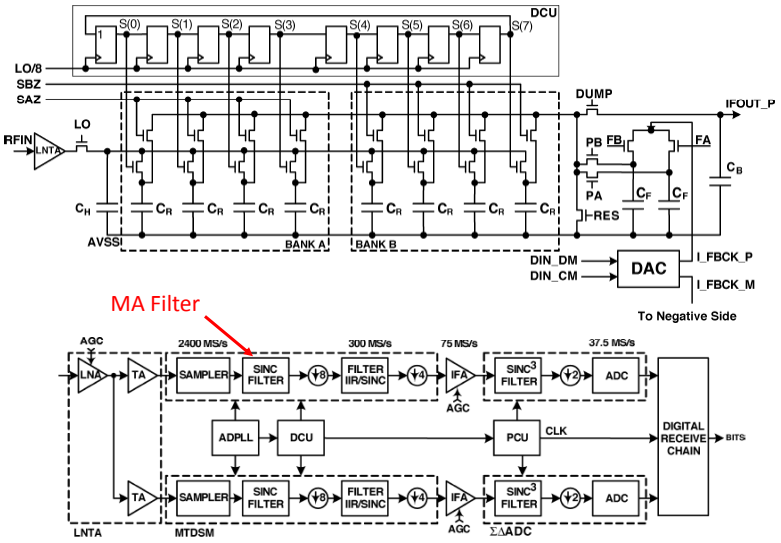
Sample-Rate Down-conversion (2)



Discrete-Time Filter in RF Rx: Summary

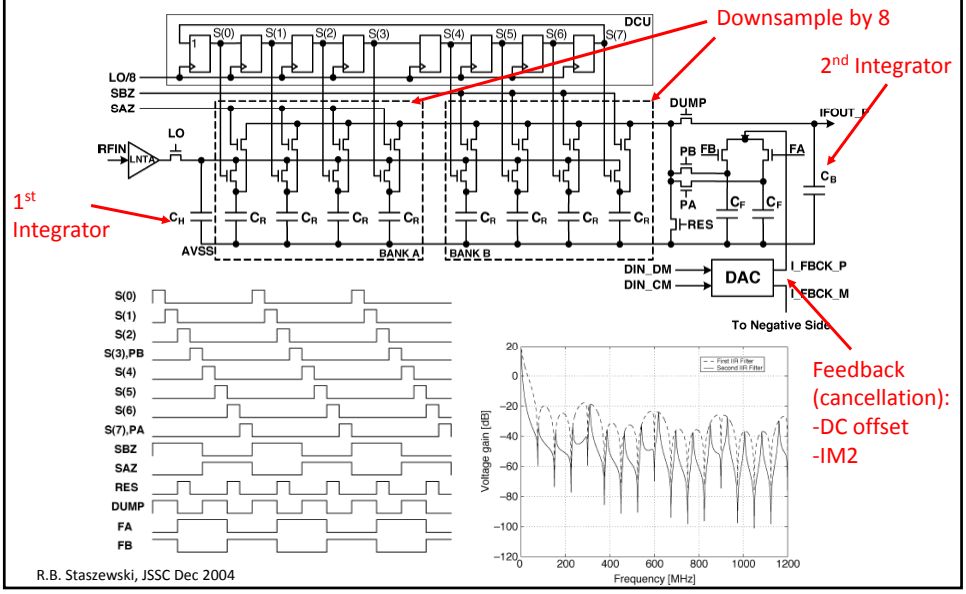
- Mixer = Sample-and-Hold
  - Main reason this technique makes sense in RF Rx
- Moving-average filter
  - Exactly what is needed prior to sample-rate reduction
- Passive switched-capacitor circuits
  - No limitation on OTA BW
- Retain all the advantage of SC filters
  - Limited pole placement due to passive nature
  - Good for low-pass filters, not for band-pass filters

TI DRP – Discrete-Time Rx



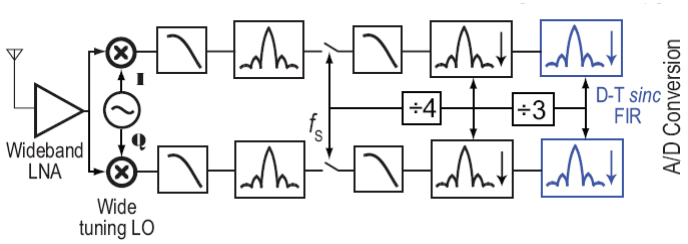
R.B. Staszewski, JSSC Dec 2004

TI DRP – Discrete-Time Rx



R.B. Staszewski, JSSC Dec 2004

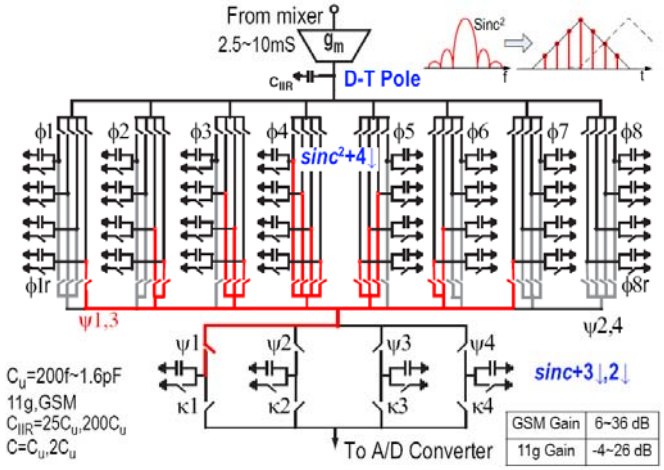
UCLA Software-Defined Rx



- Same idea: Use moving-average sampler as anti-alias filter prior to downsampling
- Need higher rejection on MA filter nulls
  - Use a triangle window, instead of a rectangular
  - Sinc² frequency response

R. Bagheri, ISSCC 2006

UCLA Software-Defined Rx

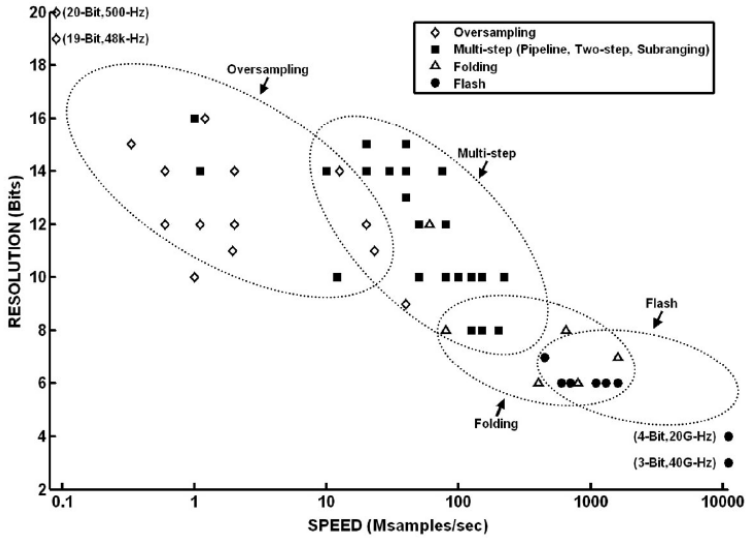


R. Bagheri, ISSCC 2006

A/D Selection for RF Receivers

- Sufficient conditions
  - Nyquist → fs = 2xBW
  - DR = SNR_{min}+PAR + '***margin'***
- Use higher sampling-rate A/D
  - Less aliasing, treat blockers as signal
  - Allocate '***margin***' for blockers
- Focus today: ΣΔ A/D converter
  - High sampling-rate
  - High dynamic-range (where it matters)

ADC Resolution vs. Speed

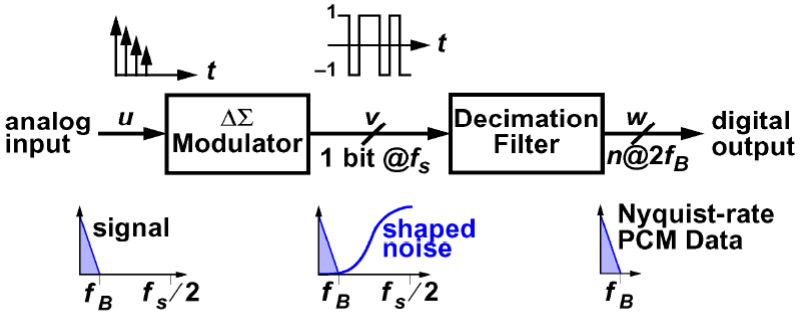


B.Kim, ISSCC 2006

Why ΣΔ A/D Converters in RF Receivers

- 'Free' anti-alias filtering
  - Actually blockers are filtered in the digital domain
- High resolution possible with low-resolution components
- Very good power efficiency (FOM)

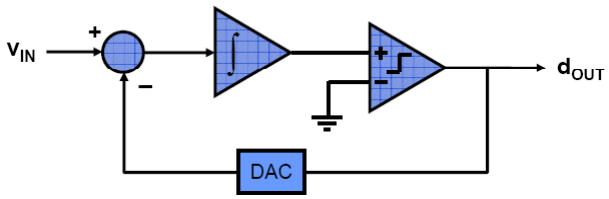
A ΔΣ ADC System

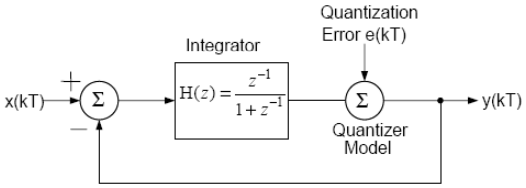


- **The ΔΣ modulator encodes (modulates) its input in such a way that the quantization noise present in the output is *shaped***
- **The decimation filter removes this noise**

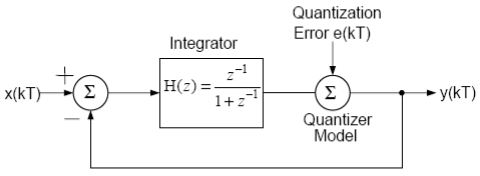
2

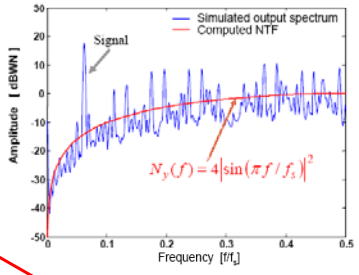
ΣΔ Modulator





ΣΔ Modulator





Signal transfer function:

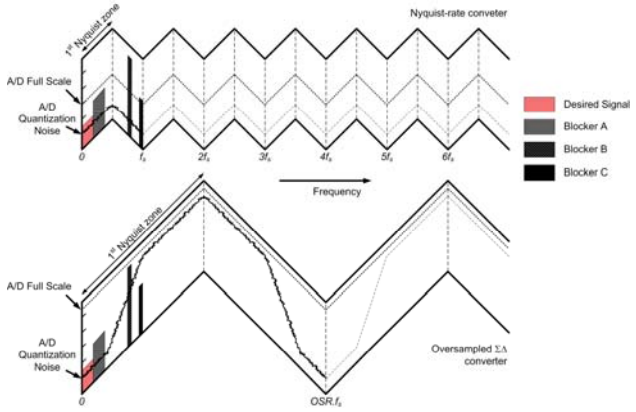
$$\text{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \quad \Rightarrow \quad \text{Delay}$$

Noise transfer function:

$$\text{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \quad \Rightarrow \quad \text{Differentiator}$$

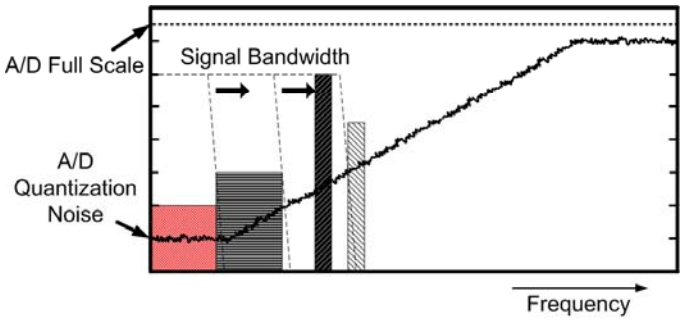
In general, filters in the ΣΔ loop shapes ***quantization noise***, not the signal

ΣΔ A/D Converters in an RF Receiver



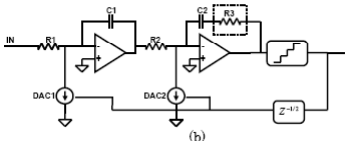
- A sigma-delta A/D is well-suited for an RF receiver:
  - ***Oversampling*** reduces aliasing
  - Low quantization noise ***only*** around signal of interest

Arbitrary Signal Bandwidth

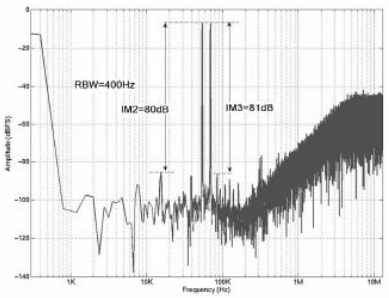


- Signal bandwidth is never explicitly defined in the analog domain
  - Large bandwidth → more quantization noise
- Final signal selection is performed in the digital domain
  - Digital filters are cheap and easily reprogrammable

ΣΔ #1: ΣΔ A/D for GSM/WCDMA



(b)

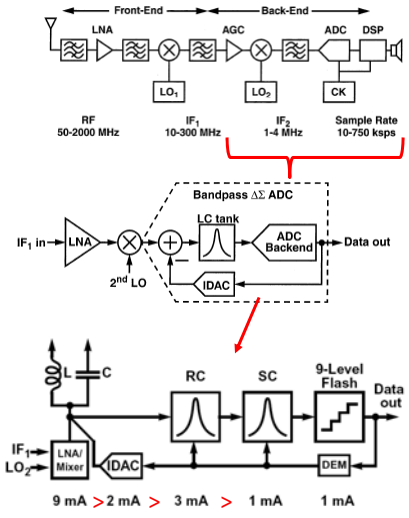


- Second-order CT SD
- Low power, small area
- Reconfigurable between GSM/WCDMA by changing clock-rate
- Most of DR is allocated for blockers

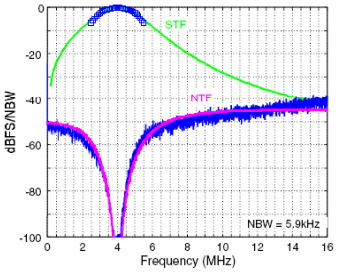
	GSM(LP)	GSM(BP)	WCDMA
Signal BW	100KHz	200KHz	1.92MHz
Dynamic Range	86dB	80dB	63dB
Peak SNR	84dB	79dB	61dB
Clock	26MHz		62.4MHz
Power	2.1mW		3.2mW
Supply voltage	1V		
Active Area	.18mm²		
Technology	CMOS 65nm		

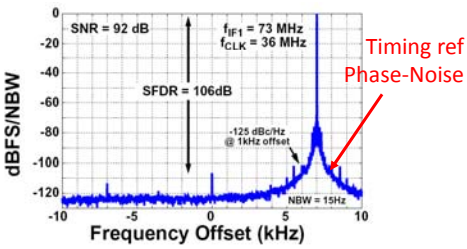
M. Vadipour, VLSI 2008

ΣΔ #2: Bandpass ΣΔ A/D



90dB @ 50mW, 333kHz BW, 10-300MHz f_{input}

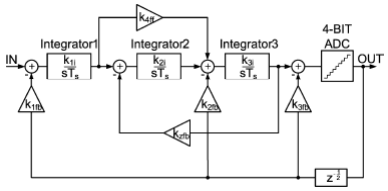




Timing ref
Phase-Noise

R. Schreier, ISSCC 2002

ΣΔ #3: Pipelined A/D Replacement



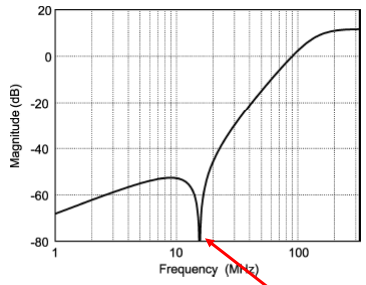


Fig. 2. Noise-transfer function (NTF) plot.

Imaginary pole (resonator) to get better NTF rejection

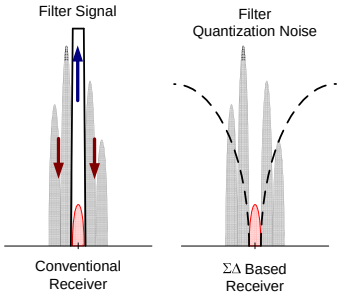
- Integrated PLL for low jitter
- 20MHz BW, 76 dB DR
  - 122 fJ/conv.step (w/o PLL)
  - 354 fJ/conv.step (w. PLL)
- Performance on par with state-of-art pipelined A/D converter
  - Anti-aliasing ***is*** free

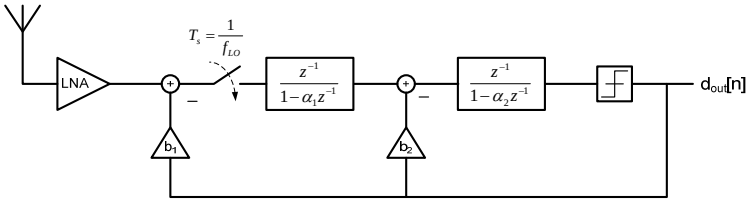
Sampling Frequency		640MHz
Conversion Rate		40MS/s
Input Range		0-20MHz
Peak SNR		76dB
THD		-78dB
Peak SNDR		74dB
ENOB		12
Process		1.2V 130nm 1P8M CMOS
Chip Area		8.6mm²
Power	Modulator	20mW
	Decimator 40MS/s	18mW
	PLL 2.56GHz	12mW
	I/O 1.8V	4mW

G. Mitteregger, JSCC December 2006

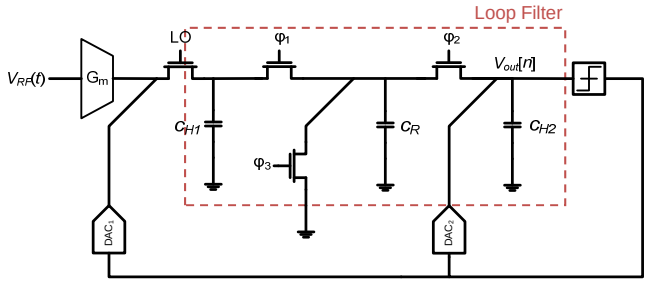
ΣΔ-Based Receiver Architecture

- It's an RF-to-digital converter
- Direct-conversion mixer
- Sample the output of mixer at f_{LO}
  - No aliasing
  - Very high oversampling ratio (OSR)
- Simple loop filter:
  - Only MOS switches, no linear amplifiers





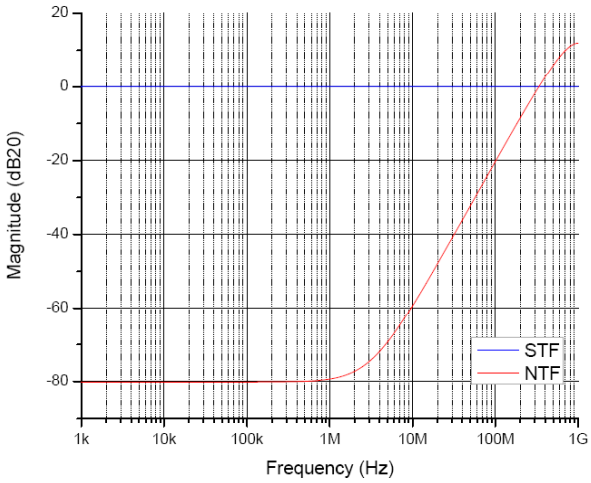
Second Order ΣΔ Modulator



- Passive, switched-capacitor loop-filter, feedback-compensated modulator
- A 1-bit quantizer and DAC is used to ensure excellent linearity

[3] F. Chen, B. Leung, "A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-in Mixer for a 10-MHz IF Input," *IEEE Journal of Solid State Circuits,* vol. 32, No. 6, pp 774-782, June 1997

ΣΔ Modulator Design



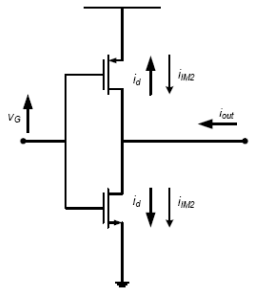
C_{H1} = 10 pF
C_{H2} = 10 pF
C_R = 100 fF
f_{LO} = 2 GHz

STF is flat across the band by design

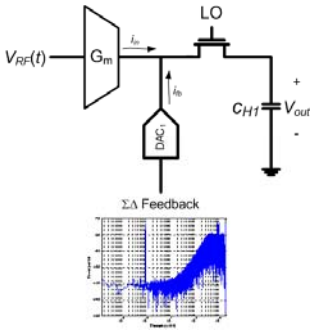
Bandwidth	SNR
2 MHz	84 dB
4 MHz	80 dB
8 MHz	74 dB
20 MHz	61 dB

GM Design: Minimizing Distortion

- Input-limited
  - Distortion due to V-to-I conversion
- ➢ Bias-point optimization



- Output-limited
  - Distortion due to excessive voltage swing
- ➢ ΣΔ FB + output load impedance



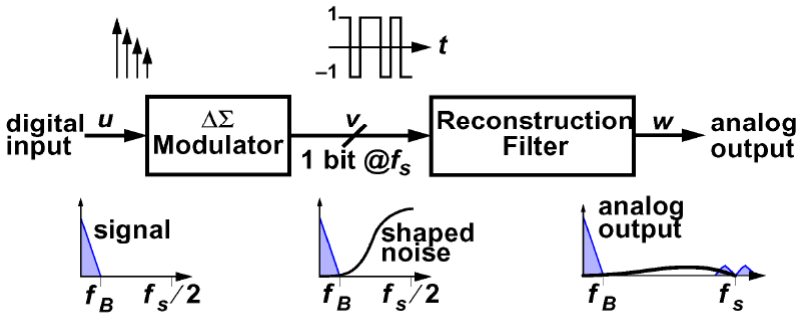
ΣΔ A/D: Summary

- ***Oversampling***
  - Spreads quantization noise over wider bandwidth
  - Less aliasing
- ***Quantization-Noise Shaping***
  - Push quantization noise away from desired BW
  - High SNR only around a narrow BW
- Enclose filters within an A→D→A feedback loop
  - Contrast with filters followed by an A/D
  - Process error signal (<< than desired signal)

Mixed-Signal in RF Tx

- Main idea: Replace PAs with DACs
  - Power efficiency (switching PAs)
  - Digital pre-distortion, correction, calibration, etc…
- Problems:
  - High-speed, high-resolution
  - Reconstruction filter
- Techniques
  - Sigma-Delta
  - Polar Modulation

A ΔΣ DAC System



- **Mathematically similar to an ADC system**
  The modulator is digital and drives a low-resolution DAC, whose output is then filtered by an analog filter to attenuate the out-of-band noise. We will concentrate on ADCs.

3

RF DACs

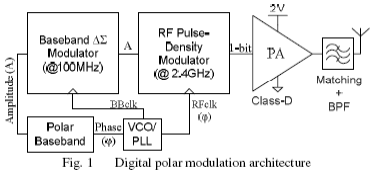
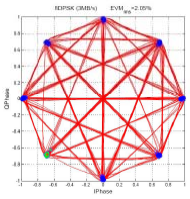
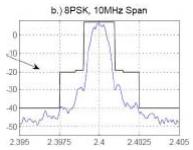


Fig. 1 Digital polar modulation architecture





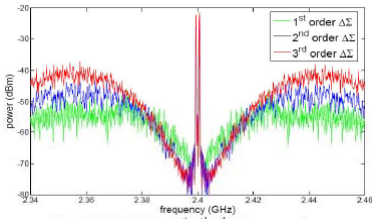
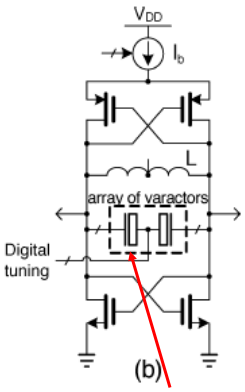


Fig. 5 ΔΣ Modulator: 1st, 2nd, 3rd-order comparison

- Cartesian → Polar
  - Phase-modulation in PLL
  - Amplitude-modulation in PA
- Use ΣΔ modulation to get good linearity out of small numbers of large switching elements
- Use matching network as reconstruction filter

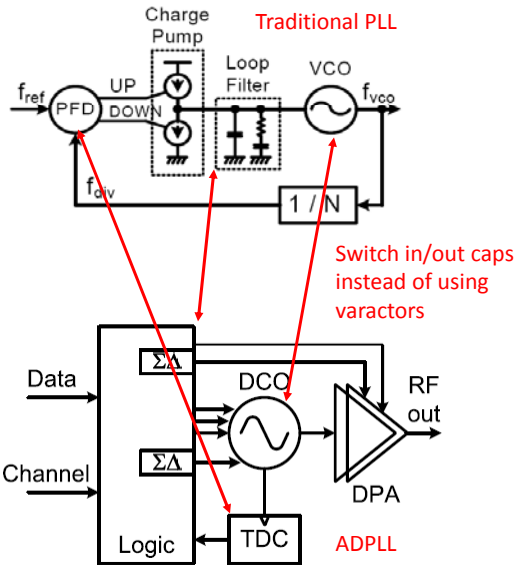
J. Stauth, CICC 2008

TI DRP: All-Digital PLL



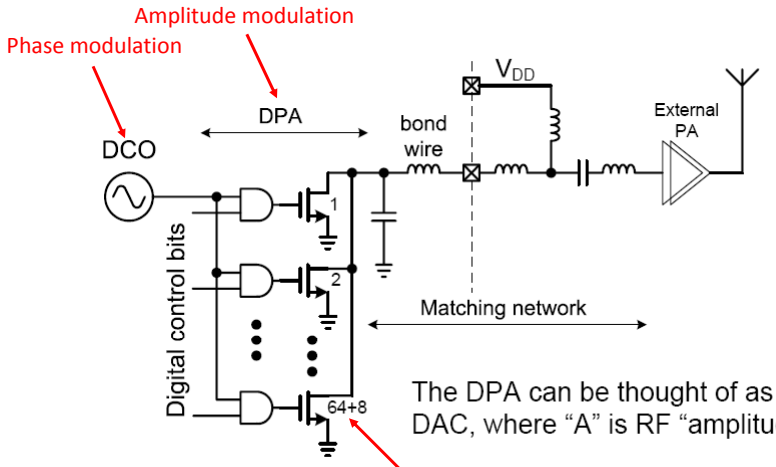
In 130nm, min gate cap is ~38 aF ≈ 23kHz @ 2.4GHz

Use ΣΔ for finer resolution



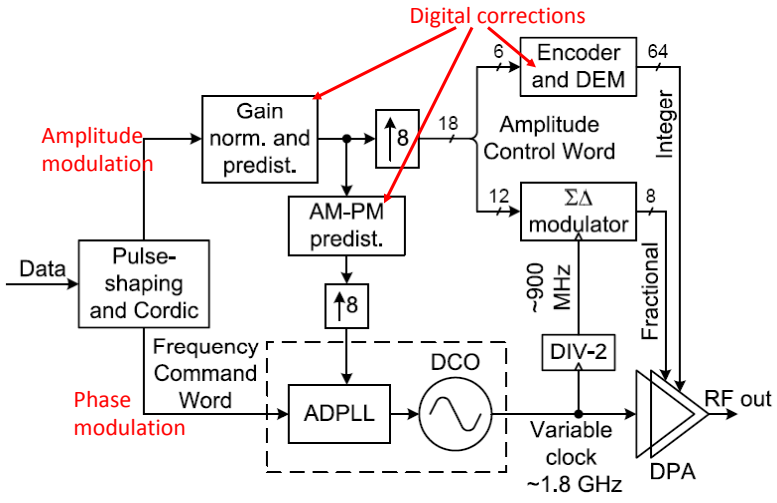
R.B. Staszewski, ISSCC 2005

TI DRP: 'Digital' PA



R.B. Staszewski, ISSCC 2005

All-Digital TX



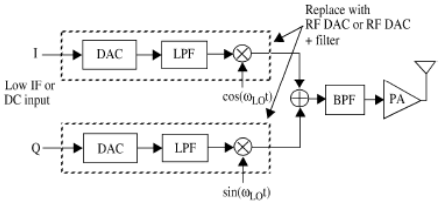
R.B. Staszewski, ISSCC 2005

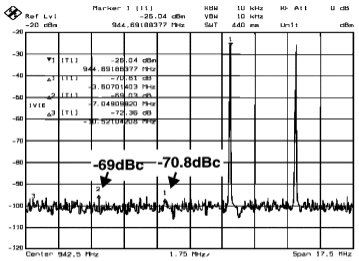
Summary

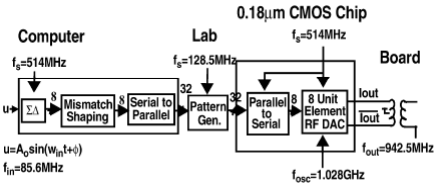
- Boundary between 'RF' and 'Mixed-signal' is diminishing in RF Transceiver design (0-5GHz)
- Lots of system optimization 'tricks' that uses a combination of RF and mixed-signal techniques
  - Transceiver design is no longer: RF designer + baseband designer + A/D designer
- Trend towards digital closer to the antenna

Extra Slides

RF DACs







S. Luschas, JSSC, Sept 2004

ΣΔ #4: ΣΔ A/D for UMTS

Feedforward Compensation

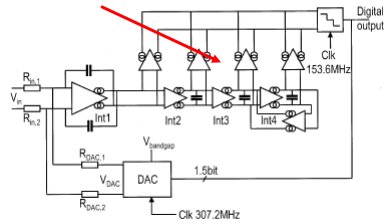
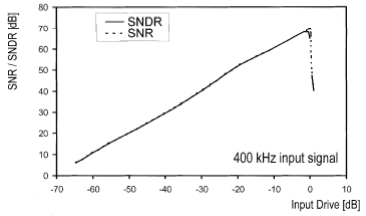
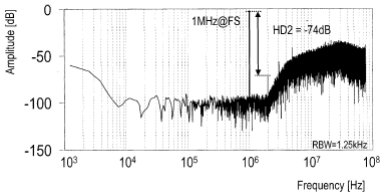


TABLE I
PERFORMANCE SUMMARY

Conversion system	Zero-IF	
ΣΔ modulator	Continuous-Time, 4th order, 1.5bit	
Sampling rate	153.6MHz	
Signal bandwidth	2MHz (single modulator)	
Oversampling ratio	40	
Input voltage range	0.5Vpp differential for a sinoid	
Dynamic range	70dB	
Total Harmonic Distortion	-74dB	
Image Rejection	>53 dB (only 6 samples measured)	
Process	1.8V, 1P, 5M, 0.18 μm CMOS	
Area and power consumption	Area [mm²]	Power@1.8V [mW]
I&Q ΣΔ modulator	2*0.12	2*3.3
PLL	0.14	3.6
Oscillator	0.029	0.72
Bandgap	0.02	0.54
	Total : 0.43 mm²	11.5 mW





70dB @ 3.3mW, 2MHz BW

R. Schreier, ISSCC 2002